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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/911,739
Filing Date: July 25, 2001
Appellant(s): YOSHIDA, TOYOHIKO

Tomoki Tanida, Limited Recognition No. L0098
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/18/2006 appealing from the Office action mailed 10/17/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1-4, 6-10, 12-16, and 18.

Claims 5, 11, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner.

Claims 1, 7 and 13 stand rejected as being unpatentable over U.S. Patent 5,881,258 ("Arya") in view of U.S. Patent 5,638,525 ("Hammond") under 35 U.S.C. §103(a).

Claims 5, 11 and 17 stand rejected as being unpatentable over Arya in view of Hammond, further in view of U.S. Patent 5,784,585 ("Denman") under 35 U.S.C. §103(a).

Claims 6, 12 and 18 stand rejected as being unpatentable over Arya in view of Hammond, further in view of U.S. Patent 5,386,547 ("Jouppi") under 35 U.S.C. §103(a).

NEW GROUND(S) OF REJECTION

Claims 6, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Augusteijn et al. (U.S. 6,292,883), further in view of Jouppi (U.S. 5,386,547).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Maintained Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 7 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Augusteijn et al. (U.S. 6,292,883), herein referred to as Augusteijn.

3. As per claim 1:

Augusteijn disclosed a data processing device with an instruction translator comprising:

A processor core: (Figure 1B, PROC 112)

And a memory interface portion (Figure 1B, preprocessor 130) arranged between said processor core and an external memory (figure1B, IM 120) mapped into a predetermined external memory space.

Said memory interface portion including a fetch circuit (FTCH 134) for receiving an address value for access to said external memory space from said processor core: (Column 11, lines 9-29 and column 7, lines 18-22)

And fetching the information at said address in said external memory, said information being an instruction nonnative to said processor an instruction native to said processor or data to be processed: (Column 7, lines 1-44)

A translator (Elements 400, 410, and 420) for translating the instruction nonnative to said processor core fetched by said fetch circuit from said external memory into the native instruction; and

A select circuit (DET 440 and FDR 136) for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not: (Figure 4, column 10, lines 36-56, column 5, line 64 to column 6, line 8. Specifically, Augusteijn states, "By determining in which region the address of the instruction to be executed lies, the converter can easily detect whether or not conversion is required (native instruction need not be converted) and which conversion means should be used for the conversion." (Col. 6, lines 4-8))

4. As per claim 7:

Claim 7 essentially recites the same limitations of claim 1. Therefore, claim 7 is rejected for the same reasons as claim 1.

5. As per claim 13:

Claim 13 essentially recites the same limitations of claim 1. Therefore, claim 13 is rejected for the same reasons as claim 1.

Maintained Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-4, 8-10 and 14-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Augusteijn et al. (U.S. 6,292,883), in view of IBM Technical Disclosure Bulletin (NN610843), herein referred to as IBM TDB.

8. As per claim 2:

Augusteijn disclosed the data processing device with the instruction translator according to claim 1, wherein said fetch circuit includes:

An address conversion circuit for effecting predetermined conversion on the address for the access from said processor core to said external memory, and a circuit for selectively applying the address sent from said processor core and the address output from said address conversion circuit to said external memory depending on whether said address is within said predetermined region or not. (The fetch circuit fetches both native (16 or 32-bit) and non-native instructions (8 bit). (Column 8, line 66 to column 9, line 12, column 9, lines 34-36 and column 10, lines 56-67) The fetch/pc counter is described as only incrementing when it is necessary, which depends on which mode the processor is in, non-native or native, it is not necessary to increment and fetch instructions as often when in the non-native mode. (Column 11, lines 41-54) However, no specific address conversion means for fetching is provided, even though

the instructions are different sizes, which one of ordinary skill in the art would recognize as a problem when it comes to addressing instructions and data in memory. However, no explicit teaching is given, and thus, Augusteijn leaves the implementation of the fetch circuit up to the designer.

IBM TDB discloses that when a processor has a native operating mode with data stored in memory at twice the size of a non-native operating mode, a simple circuit can be added to accommodate the non-native addressing instead of an elaborate program to adjust non-native addressing. The address conversion means are applied selectively depending on which mode the processor is in, native (double precision) or non-native (single precision). The circuit consists of a right shift circuit and selection hardware to determine if the right shift should be made. (Entire IBM TDB and drawing)

It would have been obvious to add the address conversion circuit taught by the IBM TDB in order to simply and effectively convert the addresses for the shorter instruction lengths of the non-native code in Augusteijn. This would allow the non-native and native instructions to be addressed in memory without the need for a complex program to convert all the addressing of the non-native instructions, and therefore there would have been motivation for one of ordinary skill in the art to combine the inventions as described above.

9. As per claim 8:

Claim 8 essentially recites the same limitations of claim 2. Therefore, claim 8 is rejected for the same reasons as claim 2.

10. As per claim 14:

Claim 14 essentially recites the same limitations of claim 2. Therefore, claim 14 is rejected for the same reasons as claim 2.

11. As per claim 3:

Augusteijn and IBM TDB disclosed the data processing device with the instruction translator according to claim 2, wherein said conversion circuit includes a division circuit for dividing the input address value by n-th (n: natural number) power of 2 and outputting the result. (The right shift performed, as taught by the IBM TDB, is a division by 2, which is a n-th power of 2, and the result is outputted. (See drawings of IBM TDB and documentation).

12. As per claim 9:

Claim 9 essentially recites the same limitations of claim 3. Therefore, claim 9 is rejected for the same reasons as claim 3.

13. As per claim 15:

Claim 15 essentially recites the same limitations of claim 3. Therefore, claim 15 is rejected for the same reasons as claim 3.

14. As per claim 4:

Augusteijn and IBM TDB disclosed the data processing device with the instruction translator according to claim 3, wherein said division circuit includes a shifter for shifting rightward the input address value by n bits. (The division by 2 that is performed, as taught by the IBM TDB, is carried out by a right-shifter. (See drawings of IBM TDB and documentation)

15. As per claim 10:

Claim 10 essentially recites the same limitations of claim 4. Therefore, claim 10 is rejected for the same reasons as claim 4.

16. As per claim 16:

Claim 16 essentially recites the same limitations of claim 4. Therefore, claim 16 is rejected for the same reasons as claim 4.

New Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 6, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Augusteijn et al. (U.S. 6,292,883), further in view of Jouppi (U.S. 5,386,547).

19. As per claim 6:

Augusteijn disclosed the data processing device with the instruction translator according to claim 1, wherein said processor core has an instruction memory (Augusteijn: Figure 1 element 120)(Element 120 is an instruction memory.).

Augusteijn is silent on how the memory device is accessed to retrieve instructions. Augusteijn is also silent on how data for instructions to operate on is received as there is no data cache shown by Augusteijn and only an instruction cache is shown where the instructions are fetched from for execution. Augusteijn is silent as to how the instruction address of the instructions to be fetched are sent to the memory

device and how the instruction data is sent back to the processor from the memory device.

Thus, Augusteijn fails to teach said data processing device further including wherein said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus; a multiplexer having inputs connected to said instruction address bus and said data address bus, respectively, for selecting said instruction address bus or said data address bus for application to said fetch circuit in response to the control signal applied from said processor core; and a second multiplexer for electrically coupling said memory bus to said instruction bus or said data bus, in response to said control signal applied from said processor core.

However, Jouppi said data processing device further including wherein said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus (Jouppi: Figure 3 elements 104, 106, 112, 114, 130, and 134, column 5 lines 1-38)(The instruction address bus is element 130 and the instruction data bus is element 112. The data address bus is element 134 and the data bus is element 104); and

A multiplexer having inputs connected to said instruction address bus and said data address bus, respectively, for selecting said instruction address bus or said data address bus for application to said fetch circuit in response to the control signal applied from said processor core (Jouppi: Figure 3 element 132, column 5 lines 35-38)(The multiplexer element 132 selects between the instruction address or data address for retrieving data from external memory. It's obvious to one of ordinary skill in the art at

the time of the invention that the fetch circuit is responsible for fetching instructions and data for the processor, and would be responsible for fetching data from external memory upon a instruction cache miss or a data cache miss.);

And a second multiplexer for electrically coupling said memory bus to said instruction bus or said data bus, in response to said control signal applied from said processor core (Jouppi: Figure 3 element 120, column 5 lines 1-38)(It's obvious to one of ordinary skill in the art at the time of the invention that since element 132 allows for instructions or data to be fetched from external memory that element 120 allows for data or instructions to be sent to the level 1 caches. Additional proof is shown from element 108 sending both data and instructions to element 120 that will send the data to either the level 1 instruction cache or the level 1 data cache.).

Augusteijn disclosed a memory system that contains an instruction memory for fetching instructions from, but is silent on how instruction data is fetched and how the data is fetched from external memory to the processor. Multiple level memories as shown in figure 3 are well-known to one of ordinary skill in the art at the time of the invention and would have been obvious to add to the processor of Augusteijn for the advantage of allowing very slow memory access times to be hidden in being able to fetch instructions and instruction data more often from faster higher level caches as shown in figure 3. The advantage of using the multiplexers such as elements 132 and 120 allow for reducing the number of busses required by the processor system. This in turn results in reduced costs for the processor. One of ordinary skill in the art would have been motivated by this advantage to implement multiplexer elements 132 and 120

on the processor of Augusteijn for the advantage of decreased costs. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement elements 120 and 132 on the processor of Augusteijn for the advantage of decreased processor costs.

20. As per claim 12:

Claim 12 essentially recites the same limitations of claim 6. Therefore, claim 12 is rejected for the same reasons as claim 6.

21. As per claim 18:

Claim 18 essentially recites the same limitations of claim 6. Therefore, claim 18 is rejected for the same reasons as claim 6.

(10) Response to Argument

22. Regarding claims 1, 7 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Augusteijn et al. (U.S. 6,292,883):

Applicant argues "Augusteijn failed to teach a select circuit for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not" for claims 1, 7, and 13.

Applicant further states:

> "According to Augusteijn et al., what DET 440 does is to detect whether or not conversion of an instruction is required (native instruction need not be converted)

> and which conversion means should be used for the conversion (see column 6, lines 4-8 of Augusteijn et al.; and paragraph 7 of the Office Action dated October 17, 2005). DET 440 is not configured to select a non-converted instruction or a converted instruction, and apply the selected one to microprocessor core 114. Therefore, the claimed select circuit and DET 440 of Augusteijn are different from each other."

This argument is not found to be persuasive for the following reason. Augusteijn disclosed the claimed limitation through the combination of elements 440 and 136 from figure 4. Element 440 is a detector element that is able to determine if the incoming instruction is an instruction that needs to be translated by any of elements 400, 410, or 420, or if the incoming instruction needs no translation and can be sent directly to element 136 (Column 10 lines 45-56). The incoming instruction comes from external memory element 120 from figure 1. The external memory is divided up into several sub ranges for storing either instructions that need to be translated or instructions that don't need to be translated (Column 10 lines 36-45). Thus, detector 440 is able to determine if the incoming instruction is to be translated or not by looking at where the instruction originated from in memory (Column 10 lines 45-56). Element 136 is then able to receive either a native instruction to the processor via element 440 or a translated instruction via elements 400, 410, or 420. Element 136 then selects from the appropriate line to send to the execution unit depending on the instruction being translated or not (Column 10 lines 45-56). Thus, elements 136 and 440 read upon the limitation with element 136 selecting a native instruction from an external memory 120 or selecting a translated instruction from elements 400, 410, or 420 and sending the instruction to the processor depending on the region of memory the instruction is in, which is determined by element 440.

instruction to the processor depending on the region of memory the instruction is in, which is determined by element 440.

23. Regarding claims 1, 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arya (U.S. 5,881,258), further in view of Hammond et al. (U.S. 5,638,525), herein referred to as Hammond.

Applicant argues "Appellant submits that demultiplexer 540 of Hammond et al. does not select translator 541 or instruction cache 520 "depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not" (see claims 1, 7 and 13). Claim 1 requires selection of "the information read from said external memory space" (including a non-converted instruction) or "the instruction prepared by translating the instruction read from said external memory space." In contrast, demultiplexer 540 of Hammond is configured to select translator 541 or instruction cache 542, but it is not configured to select a non-converted instruction or a converted instruction. Accordingly, there is a clear difference between the claimed invention and the applied combination of the references." for claims 1, 7, and 13.

This argument is found to be persuasive. The rejections for claims 1, 7, and 13 based on Arya and Hammond have been withdrawn.

24. Regarding claims 2-4, 8-10 and 14-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Augusteijn et al. (U.S. 6,292,883), in view of IBM Technical Disclosure Bulletin (NN610843).

Applicant argues "Specifically, IBM TDB does not teach, among other things, a processor having a native operation mode with data stored in memory at twice the size of a non-native operation mode, as asserted in the Office Action. Moreover, the IBM TDB disclosure does not cure the argued fundamental deficiencies of Augusteijn with respect to the rejection of parent claim 1 under 35 U.S.C. §102(e)." for claims 2, 8, and 14.

This argument is not found to be persuasive for the following reason. Claim two has no requirement for a native operation mode that stores data at twice the size of a non-native operation mode. Thus, this is a moot point as it doesn't pertain to claim 2. Furthermore, support is given for the rejection above in the claim rejections and as shown in paragraph 30, Augusteijn clearly disclosed claims 1, 7, and 13.

Applicant argues "Claims 1-2, 7-8, and 13-14 aren't supported by Augusteijn, thus claims 3-4, 9-10, and 15-16 are allowable".

This argument is not found to be persuasive for the following reason. Paragraphs 23 and 24 clearly show how Augusteijn disclosed the elements of claims 1-2, 7-8, and 13-14, in addition to the support given specifically in the claim rejections.

25. Regarding claims 5, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arya, (U.S. 5,881,258), in view of Hammond et al. (U.S. 5,638,525), further in view of Denman (U.S. 5,784,585).

Applicant argues "Claims 1, 7, and 13 aren't supported by Arya and Hammond, thus claims 5, 11, and 17 are allowable."

This argument is found to be persuasive. Claims 5, 11, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

26. Regarding claims 6, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arya (U.S. 5,881,258), in view of Hammond et al. (U.S. 5,638,525), further in view of Jouppi (U.S. 5,386,547).

Applicant argues "Claims 1, 7, and 13 aren't supported by Arya and Hammond, thus claims 6, 12, and 18 are allowable."

This argument is found to be persuasive for the following reason. However, due to the withdrawal of the claim rejections for claim 1, 7, and 13 based on Arya and Hammond, a new ground of rejection has been given for claims 6, 12, and 18 based on the same reference to specifically reject the claim 6, 12, and 18 limitations, but instead based on the Augusteijn reference instead of the Arya and Hammond combined rejection.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

JAP

Jacob A. Petranek

October 5, 2006

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